CLAIMS

1. A method for generating a mode activation signal in response to an input signal, comprising:

comparing the voltage of the input signal to the voltage of a first power supply;

comparing the voltage of the input signal to the voltage of a second power supply; and

where the voltage of the input signal exceeds the greater of the voltages of the first and second power supplies, generating in response thereto an active mode activation signal.

2. The method of claim 1 wherein generating an active mode activation signal comprises generating an active mode activation signal where the voltage of the input signal exceeds the greater of the voltages of the first and second power supplies by a voltage margin.

3. The method of claim 1 wherein comparing the voltage of the input signal to the voltage of the first power supply comprises comparing the voltage of the input signal to the voltage of a device power supply.

4. The method of claim 1 wherein comparing the voltage of the input signal to the voltage of the second power supply comprises comparing the voltage of the input signal to the voltage of an input/output power supply.

5. The method of claim 1 wherein comparing the voltage of the input signal to the voltages of the first and second power supplies comprise comparing the voltage of the input signal to the voltages of a device power supply and an input/output power supply, the voltage of the device power supply being less than the voltage of the an input/output power supply.

6. A method for generating a mode activation signal in response to an input signal, comprising determining whether the voltage of the input signal exceeds the voltage of the first power supply and the voltage of the second power supply by at least a voltage margin and generating an active mode activation signal in response thereto.

7. The method of claim 6 wherein determining whether the voltage of the input signal exceeds the voltages of the first and second power supplies comprises determining whether the voltage of the input signal exceeds the voltages of a device power supply and an input/output power supply.

8. The method of claim 6 wherein determining comprises:

comparing the voltage of the input signal to the voltage of the first power supply and generating a first true signal in response to the input signal having a voltage greater than the first power supply by the voltage margin; and

comparing the voltage of the input signal to the voltage of the second power supply and generating a second true signal in response to the input signal having a voltage greater than the second power supply by the voltage margin.

9. The method of claim 8 wherein generating an active mode activation signal comprises generating the active mode activation signal in response to the generation of the first and second true signals.

10. A method for testing a memory device having a voltage operation range including an upper and lower operating voltage, the method comprising:

setting a first power supply voltage;

setting a second power supply voltage;

applying an input signal having an input voltage to an input pin of the memory device to enter a test mode;

comparing the input voltage to the first voltage;

comparing the input voltage to the second voltage;

where the input voltage exceeds the greater of the first and second voltages by a voltage margin, generating in response thereto an active mode activation signal to enter the test mode.

11. The method of claim 10 wherein the first and second power supply voltages are set to the lower operating voltage.

12. The method of claim 10 wherein the first and second power supply voltages are set to unequal voltages.

13. The method of claim 10 wherein setting the first voltage comprises setting the voltage of a device power supply.

14. The method of claim 10 wherein setting the second voltage comprises setting the voltage of a input/output power supply.

15. The method of claim 10 wherein the voltage of the input signal is based on the voltage of the second voltage.

16. A method for testing a memory device having a voltage operation range including an upper and lower operating voltage, the method comprising:

setting a first power supply voltage;

setting a second power supply voltage;

applying an input signal having an input voltage to an input pin of the memory device to enter a test mode; and

determining whether the input voltage exceeds the voltage of the first power supply and the voltage of the second power supply by at least a voltage margin and generating an active mode activation signal in response thereto

17. The method of claim 16 wherein the first and second power supply voltages are set to the lower operating voltage.

18. The method of claim 16 wherein the first and second power supply voltages are set to unequal voltages.

19. The method of claim 16 wherein setting the first voltage comprises setting the voltage of a device power supply.

20. The method of claim 16 wherein setting the second voltage comprises setting the voltage of a input/output power supply.

21. The method of claim 16 wherein the voltage of the input signal is based on the voltage of the second voltage.

22. The method of claim 16 wherein determining comprises:

comparing the voltage of the input signal to the voltage of the first power supply and generating a first true signal in response to the input signal having a voltage greater than the first power supply by the voltage margin; and

comparing the voltage of the input signal to the voltage of the second power supply and generating a second true signal in response to the input signal having a voltage greater than the second power supply by the voltage margin.

23. The method of claim 22 wherein generating an active mode activation signal comprises generating the active mode activation signal in response to the generation of the first and second true signals.

24. An apparatus for generating a mode activation signal in response to an input signal, comprising a high-voltage detector having an input for receiving the input signal, and first and second reference inputs for receiving first and second reference voltages, respectively, the high-voltage detector further having an output at which an active mode activation signal is provided in response to the voltage of the input signal exceeding the greater of the voltages of the first and second reference voltages power supplies by a voltage margin.

25. The apparatus of claim 24 wherein the high voltage detector comprises:

a first voltage comparator having a reference input for receiving the first reference voltage and an input for receiving the input signal, the first voltage comparator further having an output at which an active output signal is provided in response to the voltage of the input signal exceeding the voltage of the first reference voltage by the first voltage margin; and

a second voltage comparator having a reference input for receiving the second reference voltage and an input for receiving the input signal, the second voltage comparator further having an output at which an active output signal is provided in response to the voltage of the input signal exceeding the voltage of the second reference voltage by the second voltage margin.

26. The apparatus of claim 25 wherein the high voltage detector further comprises a logic circuit having a first input coupled to the output of the first voltage comparator and a second input coupled to the output of the second voltage comparator, the logic gate further having an output at which an active mode activation signal is provided in response to receiving active output signals from the first and second voltage comparators.

27. The apparatus of claim 26 wherein the logic gate comprises a two-input boolean AND gate.

28. The apparatus of claim 26 wherein the first and second voltage comparators comprise:

a voltage divider having a node at which a voltage is controlled by the voltage of the respective reference voltage relative to the voltage of the input signal; and

an inverter having an input coupled to the node of the voltage divider and further having an output coupled to the output of the high voltage detector.

29. The apparatus of claim 28 wherein the first and second voltage comparator further comprise a Schmitt trigger circuit having an input coupled to the output of the inverter and an output coupled to the output of the high voltage detector.

30. The apparatus of claim 24 wherein the first and second reference voltages comprise a device power supply voltage and an input/output power supply voltage, respectively.

31. The apparatus of claim 30 wherein the device power supply voltage is less than the input/output power supply voltage.

32. The apparatus of claim 30 wherein the device power supply voltage is greater than the input/output power supply voltage.

33. The apparatus of claim 24 wherein the first and second voltage margins are approximately equal.

34. An apparatus for generating a mode activation signal in response to an input signal, comprising:

a first high voltage detector having a reference input for receiving a first reference voltage and an input for receiving the input signal, the first high voltage detector further having an output at which an active output signal is provided in response to the voltage of the input signal exceeding the voltage of the first reference voltage by a first voltage margin;

a second high voltage detector having a reference input for receiving a second reference voltage and an input for receiving the input signal, the second high voltage detector further having an output at which an active output signal is provided in response to the voltage of the input signal exceeding the voltage of the second reference voltage by a second voltage margin; and

a logic gate having a first input coupled to the output of the first high voltage detector and a second input coupled to the output of the second high voltage detector, the logic gate further having an output at which an active mode activation signal is provided in response to receiving active output signals from the first and second high voltage detectors.

35. The apparatus of claim 34 wherein the first and second high voltage detectors comprise:

a voltage divider having a node at which a voltage is controlled by the voltage of the respective reference signal relative to the voltage of the input signal; and

an inverter having an input coupled to the node of the voltage divider and further having an output coupled to the output of the high voltage detector.

36. The apparatus of claim 35 wherein the first and second high voltage detectors further comprise a Schmitt trigger circuit having an input coupled to the output of the inverter and an output coupled to the output of the high voltage detector.

37. The apparatus of claim 35 wherein the first and second reference voltages comprise a device power supply voltage and an input/output power supply voltage, respectively.

38. The apparatus of claim 37 wherein the device power supply voltage is less than the input/output power supply voltage.

39. The apparatus of claim 37 wherein the device power supply voltage is greater than the input/output power supply voltage.

40. The apparatus of claim 34 wherein the logic gate comprises a two-input boolean AND gate.

41. The apparatus of claim 34 wherein the first and second voltage margins are approximately equal.

42. A test mode entry circuit for generating a test mode activation signal in response to an input signal, comprising:

a plurality of voltage comparators, each voltage comparator having a reference input for receiving a respective reference voltage and an input for receiving the input signal, each voltage comparator further having an output at which a respective active output signal is provided in response to the voltage of the input signal exceeding the voltage of the respective reference voltage; and

a logic circuit having a corresponding plurality of inputs coupled to the output of a respective voltage comparator, the logic circuit further having an output at which an active test mode activation signal is provided in response to receiving active output signals from all of the plurality of voltage comparators.

43. The test mode entry circuit of claim 42 wherein the plurality of voltage comparators generate a respective active output signal in response to the voltage of the input signal exceeding the voltage of the respective reference voltage by a respective voltage margin.

44. The test mode entry circuit of claim 43 wherein the respective voltage margins are approximately equal.

45. The test mode entry circuit of claim 42 wherein the logic circuit comprises a logical AND gate.

46. An apparatus for generating a mode activation signal in response to an input signal, comprising:

a comparing means for comparing the voltage of the input signal to the voltages of first and second power supplies; and

a mode activation circuit coupled to the comparing means, the mode activation circuit generating an active mode activation signal in response to the voltage of the input signal exceeding the greater of the voltages of the first and second power supplies.

47. The apparatus of claim 46 wherein the mode activation circuit generates an active mode in response to the voltage of the input signal exceeding the greater of the voltages of the first and second power supplies by a voltage margin.

48. The apparatus of claim 46 wherein the first power supply comprises a device power supply.

49. The apparatus of claim 46 wherein the second power supply comprises an input/output power supply.

50. The apparatus of claim 46 wherein the first and second power supplies comprise a device power supply and an input/output power supply, respectively.

51. The apparatus of claim 50 wherein voltage of the device power supply is less than the voltage of the input/output power supply.

52. A memory device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

a mode entry circuit coupled to the control bus to generate a mode activation signal in response to an input signal, the mode entry circuit comprising a high-voltage detector having an input for receiving the input signal, and first and second reference inputs for receiving first and second reference voltages, respectively, the high-voltage detector further having an output at which an active mode activation signal is provided in response to the voltage of the input signal exceeding the greater of the voltages of the first and second reference voltages power supplies by a voltage margin.

53. The memory device of claim 52 wherein the high voltage detector of the mode entry circuit comprises:

a first voltage comparator having a reference input for receiving the first reference voltage and an input for receiving the input signal, the first voltage comparator further having an output at which an active output signal is provided in response to the voltage of the input signal exceeding the voltage of the first reference voltage by the first voltage margin; and

a second voltage comparator having a reference input for receiving the second reference voltage and an input for receiving the input signal, the second voltage comparator further having an output at which an active output signal is provided in response to the voltage of the input signal exceeding the voltage of the second reference voltage by the second voltage margin.

54. The memory device of claim 53 wherein the high voltage detector further comprises a logic circuit having a first input coupled to the output of the first voltage comparator and a second input coupled to the output of the second voltage comparator, the logic gate further having an output at which an active mode activation signal is provided in response to receiving active output signals from the first and second voltage comparators.

55. The memory device of claim 54 wherein the logic gate comprises a two-input boolean AND gate.

56. The memory device of claim 53 wherein the first and second voltage comparators comprise:

a voltage divider having a node at which a voltage is controlled by the voltage of the respective reference voltage relative to the voltage of the input signal; and

an inverter having an input coupled to the node of the voltage divider and further having an output coupled to the output of the high voltage detector.

57. The memory device of claim 56 wherein the first and second voltage comparator further comprise a Schmitt trigger circuit having an input coupled to the output of the inverter and an output coupled to the output of the high voltage detector.

58. The memory device of claim 52 wherein the first and second reference voltages comprise a device power supply voltage and an input/output power supply voltage, respectively.

59. The memory device of claim 58 wherein the device power supply voltage is less than the input/output power supply voltage.

60. The memory device of claim 58 wherein the device power supply voltage is greater than the input/output power supply voltage.

61. The memory device of claim 52 wherein the first and second voltage margins are approximately equal.

62. A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

a mode entry circuit coupled to the control bus to generate a mode activation signal in response to an input signal, the mode entry circuit comprising a high-voltage detector having an input for receiving the input signal, and first and second reference inputs for

receiving first and second reference voltages, respectively, the high-voltage detector further having an output at which an active mode activation signal is provided in response to the voltage of the input signal exceeding the greater of the voltages of the first and second reference voltages power supplies by a voltage margin.

63. The computer system of claim 62 wherein the high voltage detector of the mode entry circuit comprises:

a first voltage comparator having a reference input for receiving the first reference voltage and an input for receiving the input signal, the first voltage comparator further having an output at which an active output signal is provided in response to the voltage of the input signal exceeding the voltage of the first reference voltage by the first voltage margin; and

a second voltage comparator having a reference input for receiving the second reference voltage and an input for receiving the input signal, the second voltage comparator further having an output at which an active output signal is provided in response to the voltage of the input signal exceeding the voltage of the second reference voltage by the second voltage margin.

64. The computer system of claim 63 wherein the high voltage detector further comprises a logic circuit having a first input coupled to the output of the first voltage comparator and a second input coupled to the output of the second voltage comparator, the logic gate further having an output at which an active mode activation signal is provided in response to receiving active output signals from the first and second voltage comparators.

65. The computer system of claim 64 wherein the logic gate comprises a two-input boolean AND gate.

66. The computer system of claim 63 wherein the first and second voltage comparators comprise:

a voltage divider having a node at which a voltage is controlled by the voltage of the respective reference voltage relative to the voltage of the input signal; and

an inverter having an input coupled to the node of the voltage divider and further having an output coupled to the output of the high voltage detector.

67. The computer system of claim 66 wherein the first and second voltage comparator further comprise a Schmitt trigger circuit having an input coupled to the output of the inverter and an output coupled to the output of the high voltage detector.

68. The computer system of claim 62 wherein the first and second reference voltages comprise a device power supply voltage and an input/output power supply voltage, respectively.

69. The computer system of claim 68 wherein the device power supply voltage is less than the input/output power supply voltage.

70. The computer system of claim 68 wherein the device power supply voltage is greater than the input/output power supply voltage.

71. The computer system of claim 62 wherein the first and second voltage margins are approximately equal.